WHAT IS CLAIMED IS:

1. A system for providing frequency domain synchronization for a single carrier signal, said system comprising:

a synchronization circuit that is capable of receiving said single carrier signal, and capable of obtaining a coarse frequency estimate of said single carrier signal, and capable of obtaining a fine frequency estimate of said single carrier signal.

2. The system as claimed in Claim 1 where said single carrier signal is a vestigial sideband signal.

3. The system as claimed in Claim 1 wherein said synchronization circuit is capable of obtaining a coarse frequency estimate of said single carrier signal by locating a pilot carrier signal on an average power spectrum of said single carrier signal.

4. The system as claimed in Claim 1 wherein said synchronization circuit is capable of obtaining a fine frequency estimate of said single carrier signal using the frequency error Δf_p where Δf_p is given by the equation:

$$\Delta f_p = [\ 1 / (2\pi\ N\ T_s)\ ]\ [\ \mathrm{Arg}\ [\ X_{pr,q}(0)\ /\ X_{pr,q+1}(0)\ ]\ ]$$

where $[\ 1 / (N\ T_s)\ ]$ is the frequency spacing, and where T_s is the sampling period, and where $X_{pr}(0)$ is the transmitted signal with constant frequency error in the zeroth bin, and where $\mathrm{Arg}\ [\ X_{pr,q}(0)\ /\ X_{pr,q+1}(0)]$ is the phase of a pilot carrier signal in the zeroth bin.

5. The system as claimed in Claim 1 wherein said synchronization circuit further comprises a three state machine for obtaining a final frequency estimate of said single carrier signal, said three state machine capable of obtaining a first frequency estimate, and capable of obtaining a second frequency estimate with a known fixed frequency estimate of a positive one fourth bin spacing, and capable of obtaining a third frequency estimate with a known fixed frequency estimate of a negative one fourth bin spacing.

6. The system as claimed in Claim 5 wherein said three state machine is capable of determining which two of the three frequency estimates are closest in value, and capable of obtaining an average of the two closest frequency estimates, and capable of calculating said final frequency estimate of said single carrier signal by adding one fourth of a bin spacing to said average of the two closest frequency estimates.

7. The system as claimed in Claim 5 where said three state machine is capable of obtaining said first, second, and third frequency estimates of a single carrier signal by obtaining a coarse frequency estimate of said single carrier signal by locating a pilot carrier signal on an average power spectrum of said single carrier signal, and by obtaining a fine frequency estimate of said single carrier signal using the frequency error Δf_p where Δf_p is given by the equation:

$$\Delta f_p = [\ 1 / (2\pi\ N\ T_s)\ ]\ [\ \mathrm{Arg}\ [\ X_{pr,q}(0)\ /\ X_{pr,q+1}(0)\ ]\ ]$$

where $[\ 1 / (N\ T_s)\ ]$ is the frequency spacing, and where T_s is the sampling period, and where $X_{pr}(0)$ is the transmitted signal with constant frequency error in the zeroth bin, and where $\mathrm{Arg}\ [\ X_{pr,q}(0)\ /\ X_{pr,q+1}(0)]$ is the phase of a pilot carrier signal in the zeroth bin.

8. The system as claimed in Claim 7 wherein said synchronization circuit has a linear transfer function.

9. A system for providing frequency domain synchronization for a single carrier signal, said system comprising:

a synchronization circuit comprising a Fast Fourier Transformer, a coarse frequency estimate circuit coupled to an output of said Fast Fourier Transformer, and a fine frequency estimate and phase estimate circuit coupled to an output of said Fast Fourier Transformer, and

a DC estimator circuit capable of being coupled to said fine frequency estimate and phase estimate circuit in place of said output of said Fast Fourier Transformer, said DC estimator circuit capable of providing a time domain DC estimate to said fine frequency estimate and phase estimate circuit.

10. The system as claimed in Claim 9 wherein said DC estimator circuit calculates said time domain DC estimate, DC_{NEW}, from the equation:

$$DC_{NEW} = FFT\ (0) - Input\ (N) + Input\ (0)$$

where FFT (0) is a processed DC estimate, and where Input (N) is an input sample received N time periods earlier, and where Input(0) is a current input sample.

11. The system as claimed in Claim 10 wherein said DC estimator circuit receives the value of Input (N) from an output of a circular input buffer for said Fast Fourier Transformer, and wherein said DC estimator circuit receives the value of Input (0) from an output of a sample rate converter, and wherein said DC estimator circuit receives the value of FFT(0) from an output of an adder that adds the outputs of said coarse frequency estimate circuit and said fine frequency estimate and phase estimate circuit.

12. A method for providing frequency domain synchronization for a single carrier signal, said method comprising the steps of:

receiving a single carrier signal in a synchronization circuit;

obtaining a coarse frequency estimate of said single carrier signal in said synchronization circuit; and

obtaining a fine frequency estimate of said single carrier signal in said synchronization circuit.

13. The method as claimed in Claim 12 wherein said single carrier signal is a vestigial sideband signal.

14. The method as claimed in Claim 12 where said step of obtaining a coarse frequency estimate of said single carrier signal in said synchronization circuit comprises the step of:

locating a pilot carrier signal on an average power spectrum of said single carrier signal.

15. The method as claimed in Claim 12 where said step of obtaining a fine frequency estimate of said single carrier signal in said synchronization circuit comprises the step of:

calculating said fine frequency estimate using the frequency error Δf_p where Δf_p is given by the equation:

$$\Delta f_p = [\ 1 / (2\pi\ N\ T_s)\ ]\ [\ \mathrm{Arg}\ [\ X_{pr,q}(0)\ /\ X_{pr,q+1}(0)\ ]\ ]$$

where $[\ 1 / (N\ T_s)\ ]$ is the frequency spacing, and where T_s is the sampling period, and where $X_{pr}(0)$ is the transmitted signal with constant frequency error in the zeroth bin, and where $\mathrm{Arg}\ [\ X_{pr,q}(0) / X_{pr,q+1}(0)]$ is the phase of a pilot carrier signal in the zeroth bin.

16. The method as claimed in Claim 12 further comprising the steps of:

obtaining in a three state machine a first frequency estimate of said single carrier signal;

obtaining in said three state machine a second frequency estimate of said single carrier signal with a known fixed frequency estimate of a positive one fourth bin spacing; and

obtaining in said three state machine a third frequency

estimate of said single carrier signal with a known fixed frequency estimate of a negative one fourth bin spacing.

17. The method as claimed in Claim 16 further comprising the steps of:

determining which two of said three frequency estimates are closest in value;

obtaining an average of the two closest frequency estimates; and

calculating a final frequency estimate of said single carrier signal by adding one fourth of a bin spacing to said average of the two closest frequency estimates.

18. The method as claimed in Claim 16 further comprising the steps of:

obtaining said first, second and third frequency estimates of a single carrier signal by

obtaining a coarse frequency estimate of said single carrier signal by locating a pilot carrier signal on an average power spectrum of said single carrier signal; and by

obtaining a fine frequency estimate of said single carrier signal obtaining a fine frequency estimate of said single carrier signal using the frequency error Δf_p where Δf_p is given by the equation:

$$\Delta f_p = [\ 1\ /(2\pi\ N\ T_s)\ ]\ [\ \mathrm{Arg}\ [\ X_{pr,q}(0)\ /\ X_{pr,q+1}(0)\ ]\ ]$$

where $[\ 1\ /\ (N\ T_s)\ ]$ is the frequency spacing, and where T_s is the sampling period, and where $X_{pr}(0)$ is the transmitted signal with constant frequency error in the zeroth bin, and where $\mathrm{Arg}\ [\ X_{pr,q}(0)\ /\ X_{pr,q+1}(0)]$ is the phase of a pilot carrier signal in the zeroth bin.

19. The method as claimed in Claim 18 wherein said synchronization circuit has a linear transfer function.

20. A method for providing frequency domain synchronization for a single carrier signal, said method comprising the steps of:

generating a time domain DC estimate in a DC estimator circuit; and

providing said time domain DC estimate to a fine frequency estimate and phase estimate circuit.

21. The method as claimed in Claim 20 wherein said time domain DC estimate is provided to said fine frequency estimate and phase estimate circuit by

switching an input of said fine frequency estimate and phase estimate circuit from an output of a Fast Fourier Transformer to an output of said DC estimator circuit.

22. The method as claimed in Claim 20 wherein the step of generating said time domain DC estimate in said DC estimator circuit comprises the step of:

calculating said time domain DC estimate, DC_{NEW}, from the equation:

$$DC_{NEW} = FFT(0) - Input(N) + Input(0)$$

where FFT (0) is a processed DC estimate, and where Input (N) is an input sample received N time periods earlier, and where Input(0) is a current input sample.

23. The method as claimed in Claim 22 comprising the steps of:

providing the value of Input(N) to said DC estimator circuit from an output of a circular input buffer for a Fast Fourier Transformer;

providing the value of Input(0) to said DC estimator circuit from an output of a sample rate converter; and

providing the value of FFT(0) from an output of an adder that adds the outputs of a coarse frequency estimate circuit and said fine frequency estimate and phase estimate circuit.